TOTAL IONIZING DOSE CHARACTERIZATION RESULTS OF ACTEL PROASIC3, PROASIC3L, AND IGLOO FLASH-BASED FIELD PROGRAMMABLE GATE ARRAYS

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Overview

- Background and Motivations
- Device Overview
- Test Setup/Approach
- Test Results
- Mitigation Discussion
- Conclusions/Future Work

Background and Motivations

- Funded by the NASA Electronic Parts and Packaging Program (NEPP) in an effort to enable reconfigurable FPGAs to be used in space applications by characterizing and mitigating radiation issues.
- ProASIC3 family of FPGAs are 130nm flash-based (non-volatile and reconfigurable) devices
- Although the SEE response (SET characterization) has been thoroughly explored [1]-[3], the TID failure modes have had less characterization.

Device Overview

- Devices tested: Commercial A3P600/L-FG484 and AGL600-FG484 (See App. for lot/date codes).
- Device Attributes:
  - 1.5 V core (A3P600); 1.2 or 1.5 V core (A3P600L and AGL600)
  - 600K system gates and 13,824 DFlip-Flops
  - 108K RAM bits and 1K Flash ROM bits
  - 1 Phase Locked Loop
  - 4 I/O Banks with 235 single ended I/O and 60 differential I/O pairs
  - Temperature Grade: C, I

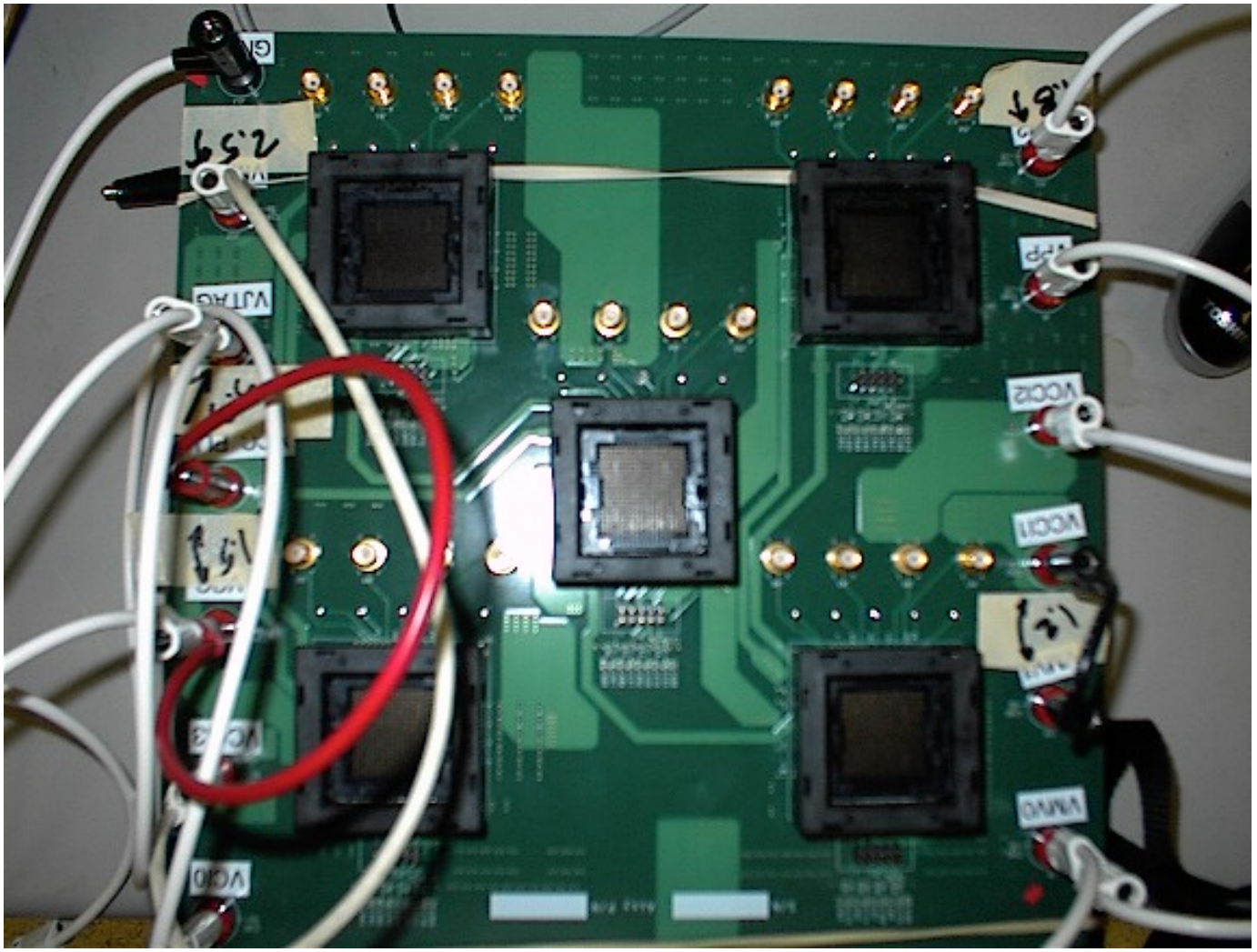
Test Setup—FPGA Design

- A 2000 stage inverter chain (propagation delay) and a 2000 stage shift register chain (at speed dynamic test)
- 4 banks set to different IO standards (1.2, 1.5, 2.5, and 3.3 V) driving 0, 1, or an I/O loop.

Test Setup-Data Acquisition

- Parametrics acquired with ETS-300 and Actel socketed test board
- Automatic measurements of supply leakage currents, IIH, IIL, VIH, VIL, VOH, VOL, IOH, IOL, IOZH, IOZL, TPDLH, and TPDHL

Test Setup-Hardware



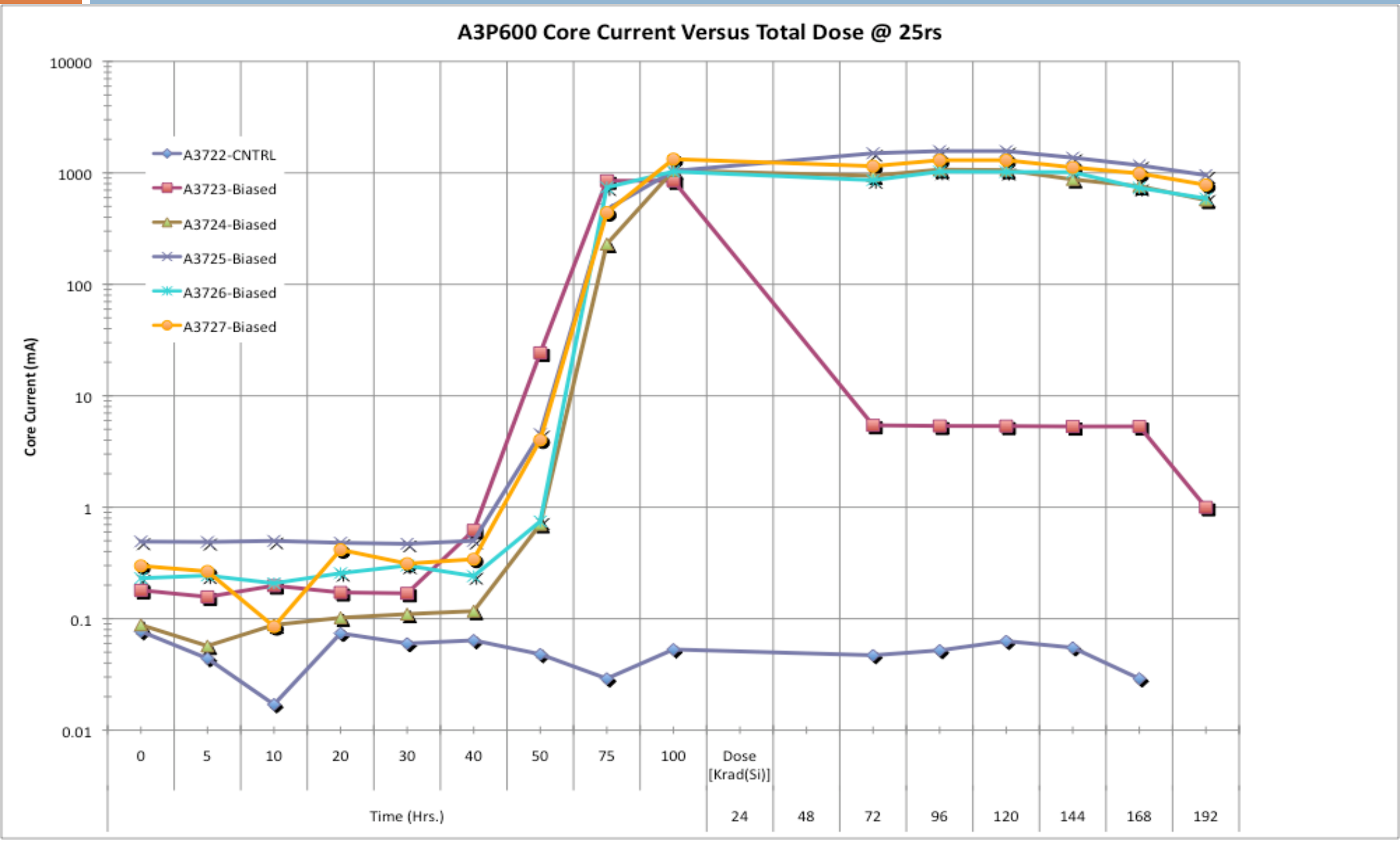
Test Conditions

- All devices were irradiated with steps of 5k, 10k, 20k, 30k, 40k, 50k, 75k, and 100kRad(Si) at a dose rate of 25 Rad(Si)/sec at room temperature using JPL's Co-60 source.
- All devices were statically biased with a 1.5V core and appropriate I/O voltages during irradiations
- Functional measurements taken with a programmable 660MHz pulse generator and 500MHz oscilloscope.

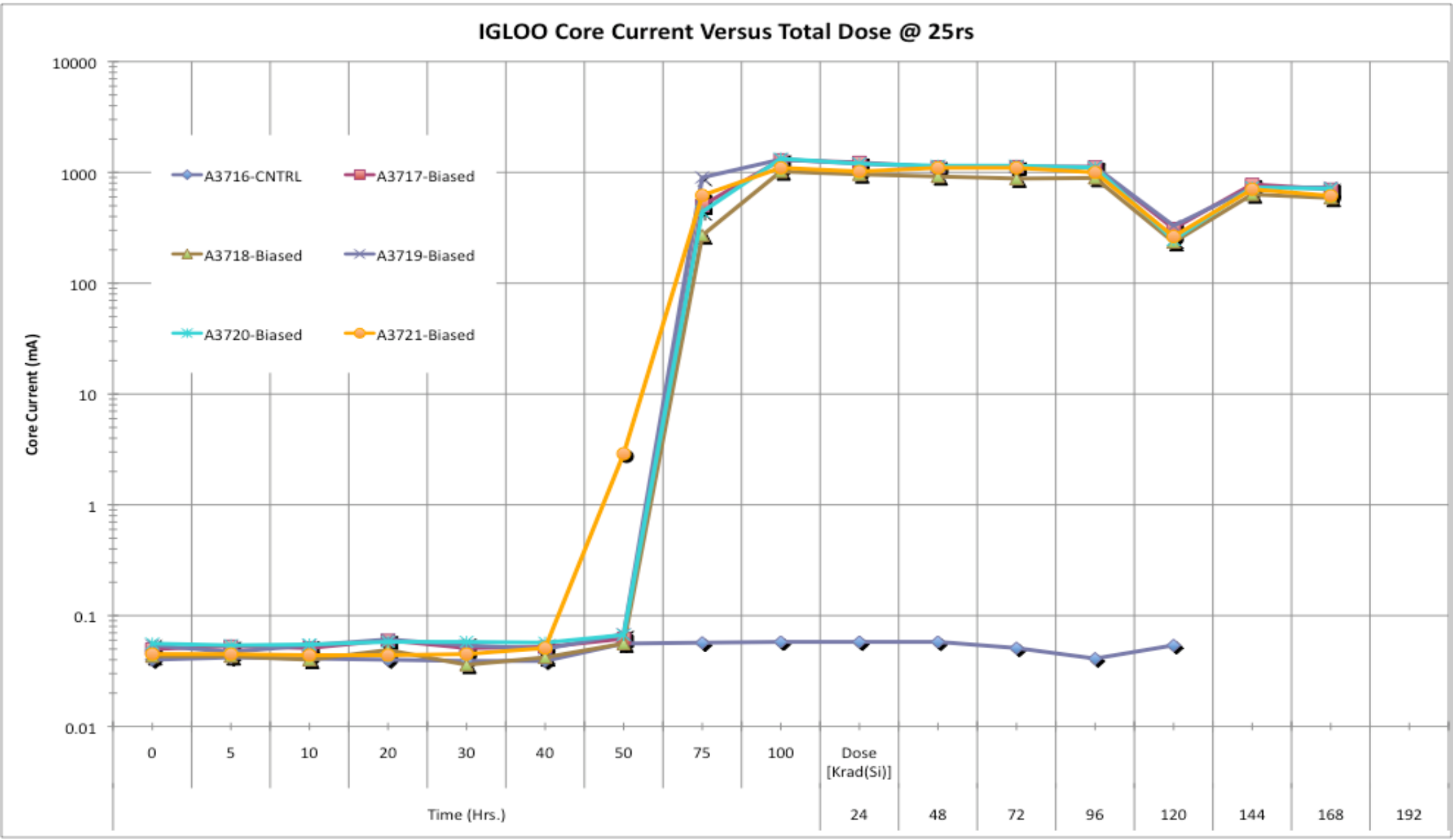
Anneal Conditions

- Anneal measurements taken every 24 hours for 1 week.
- All devices were unbiased and stored at room temperature during anneal period
- After the 1 week anneal, the devices were biased and baked at 85°C for 24 hours and final anneal measurements were made.

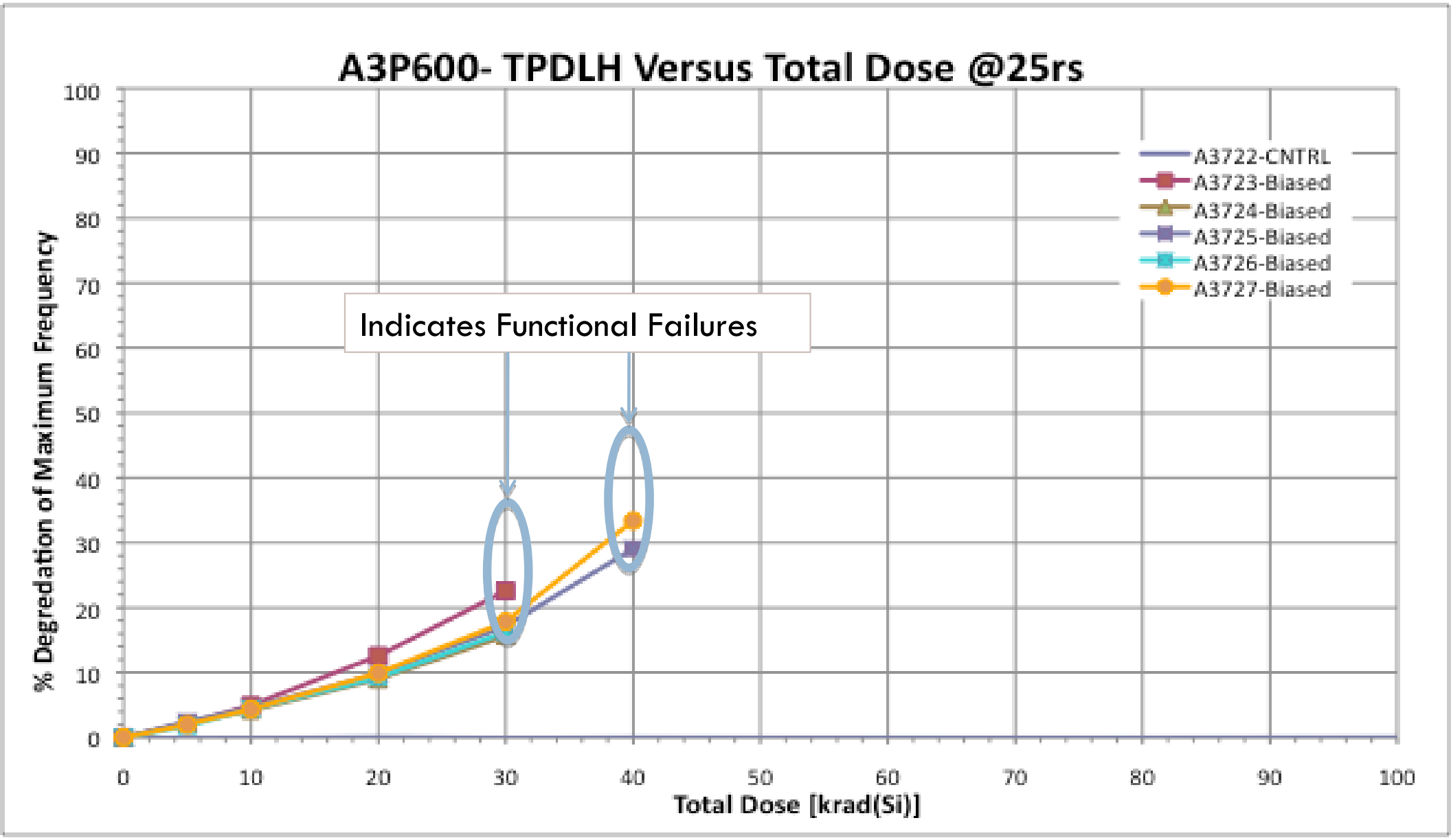
Test Results-Core Current



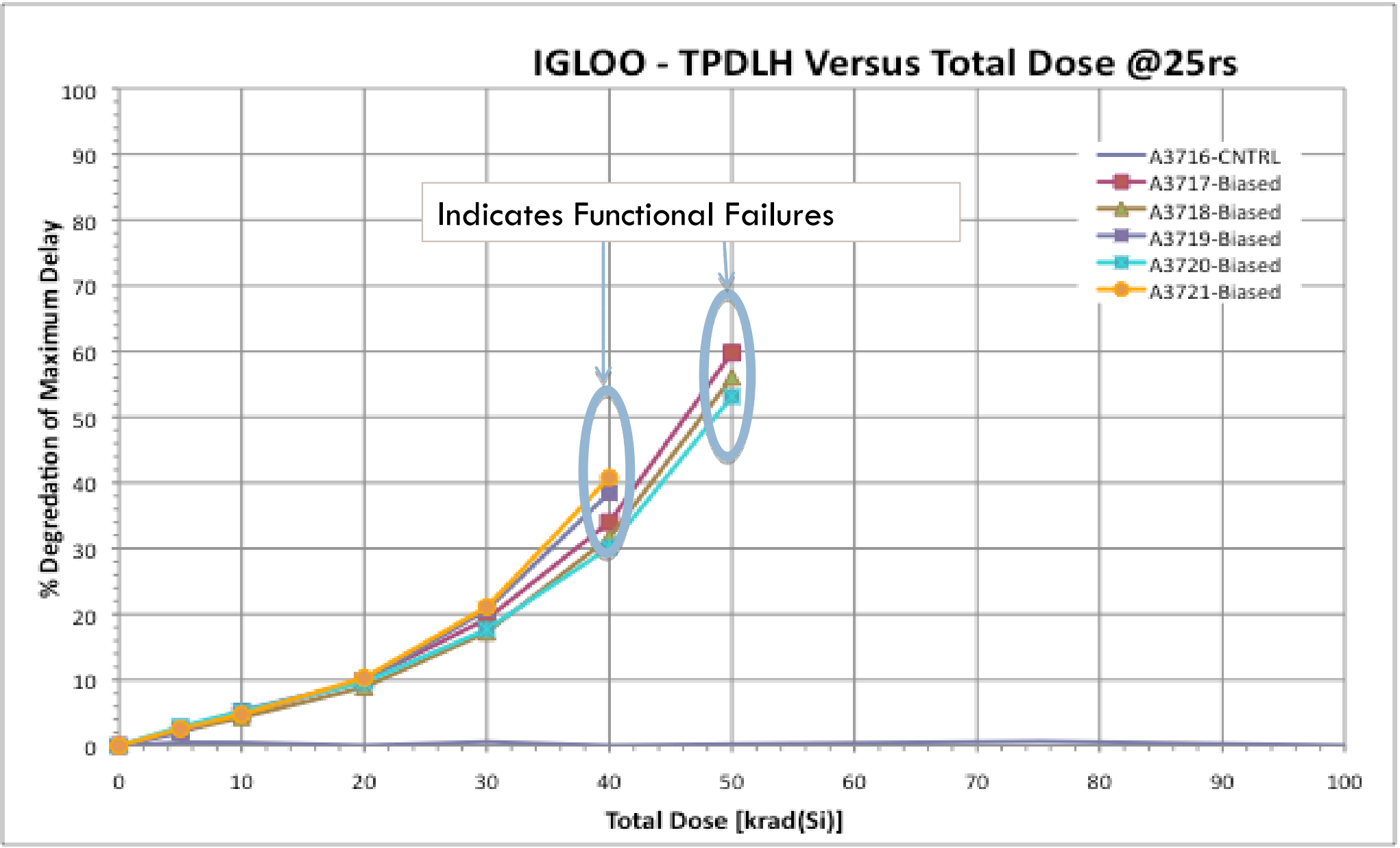
Test Results-Core Current



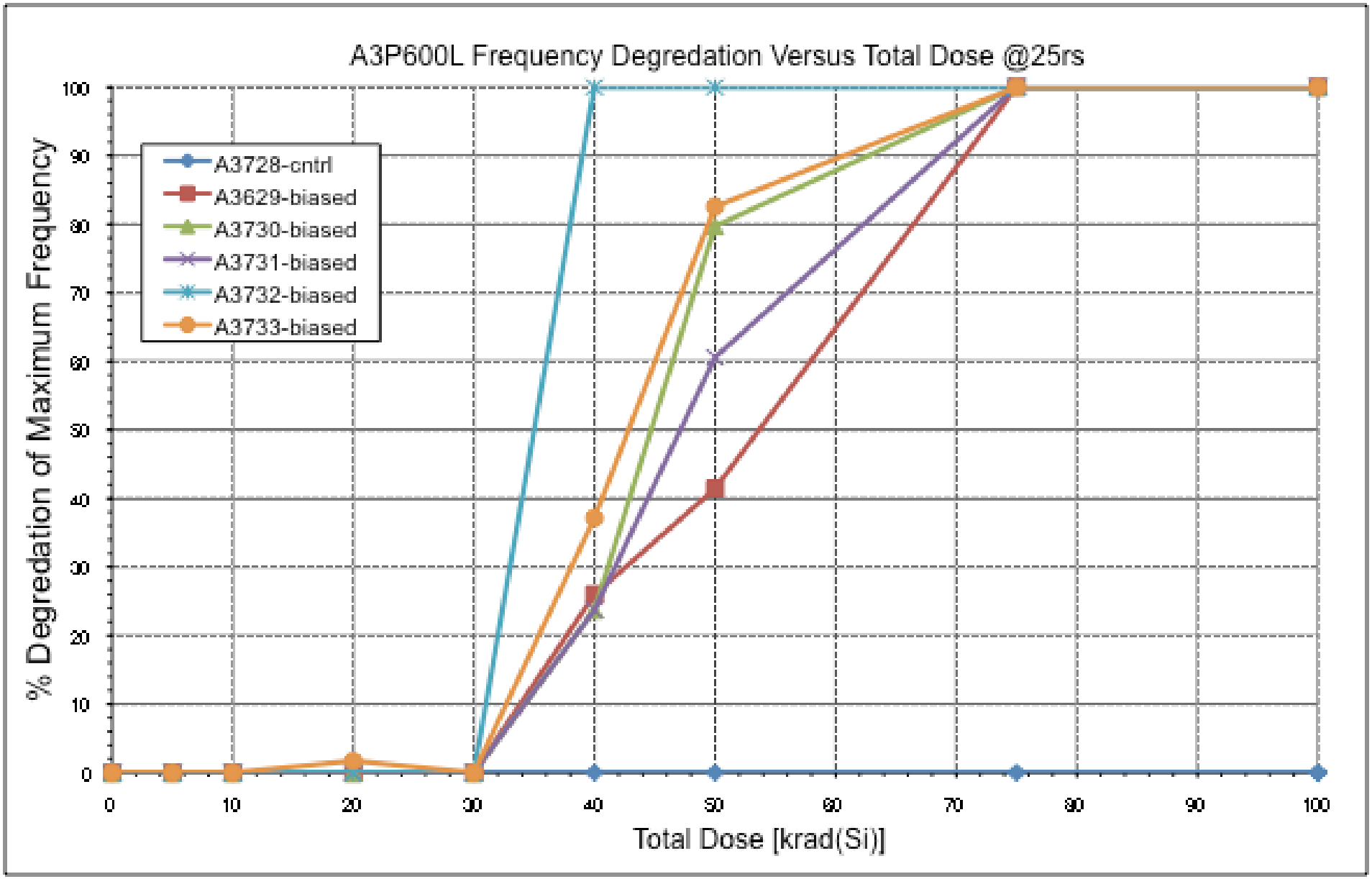
Test Results-Propagation Delay



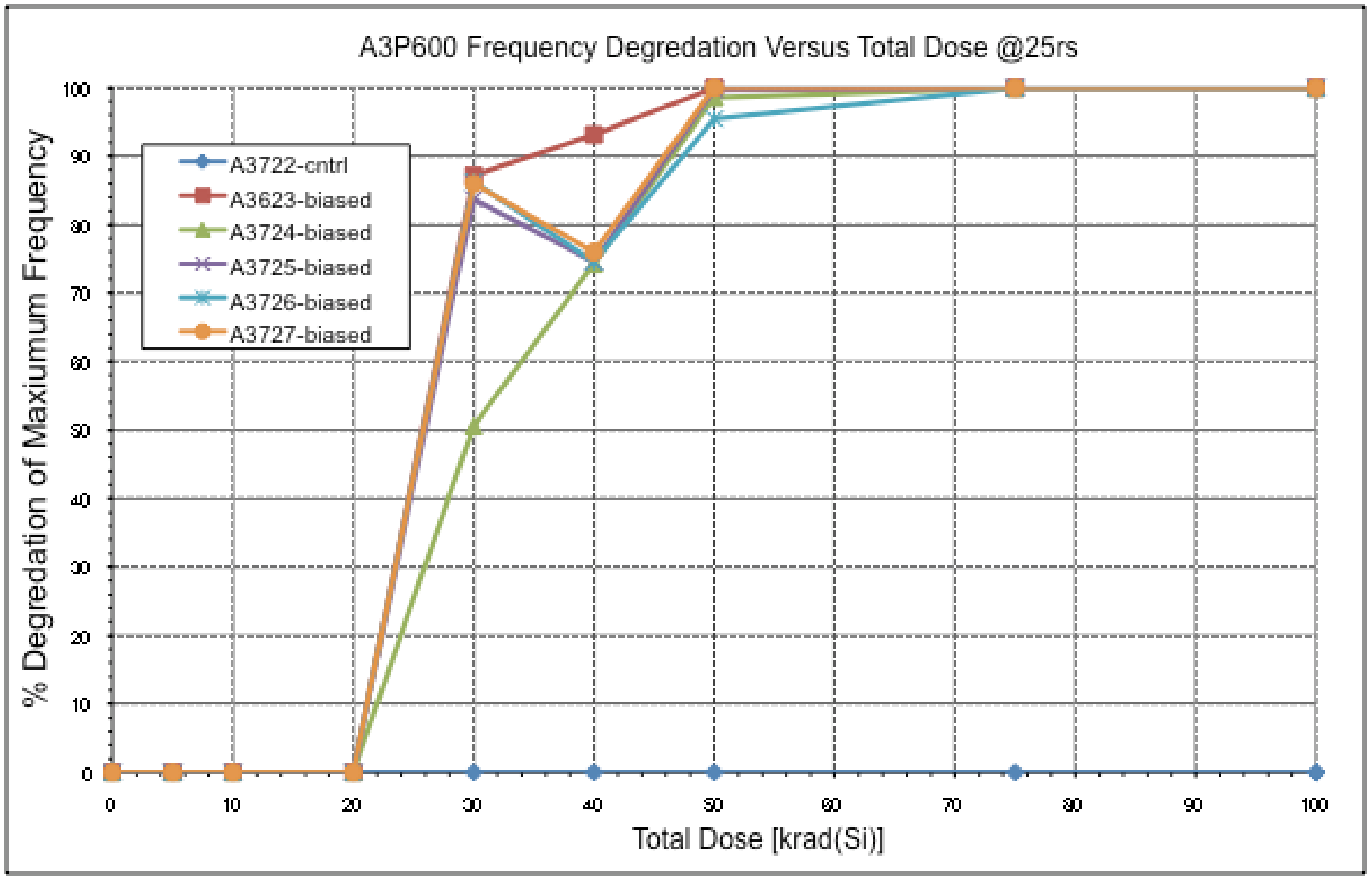
Test Results-Propagation Delay



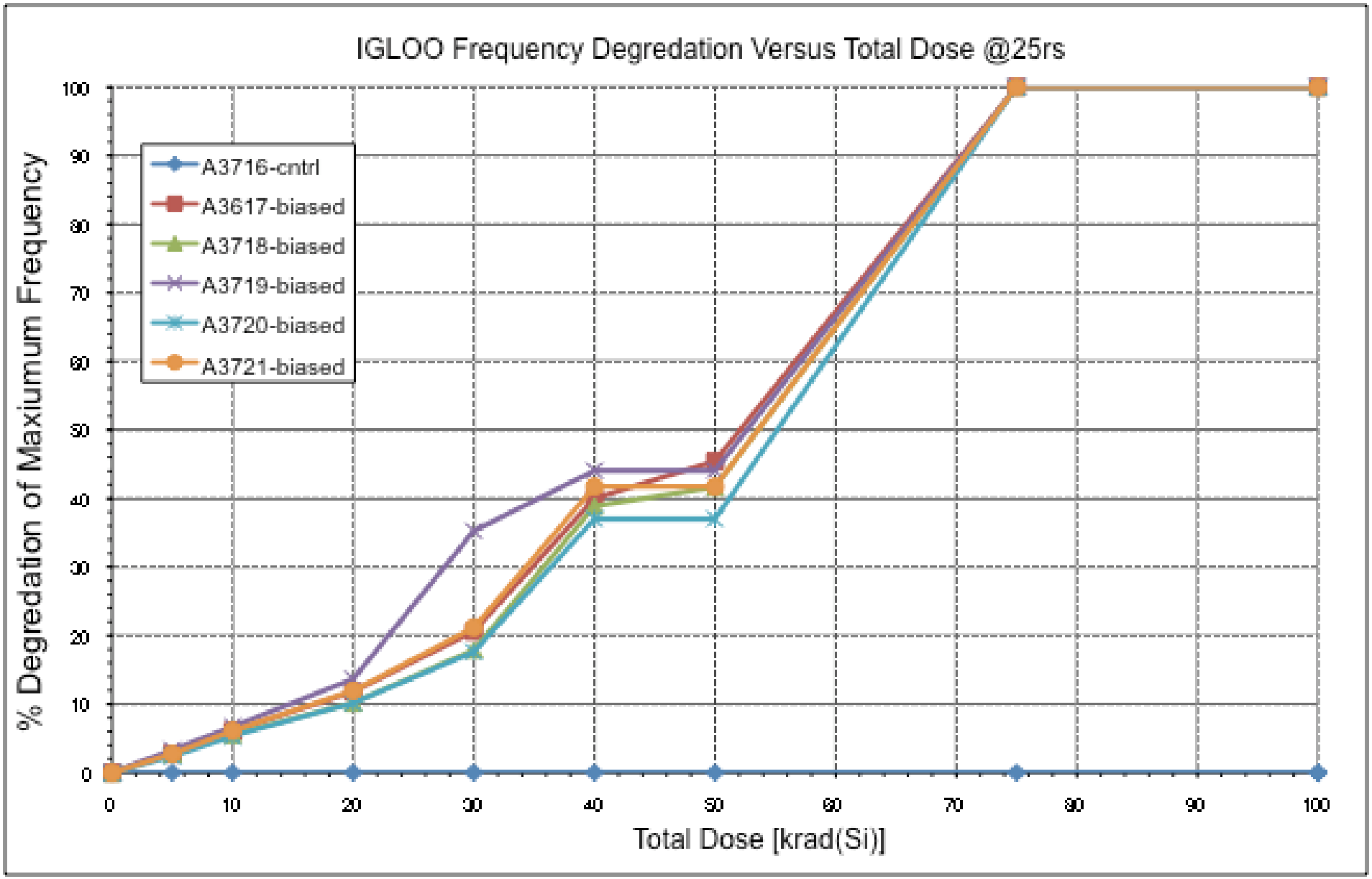
Test Results-Functional Degradation



Test Results-Functional Degradation



Test Results-Functional Degradation



Possible Mitigation and Future Work

- Full report to be available on the NASA NEPP [4] and JPL parts [5] website.
- Possible path to a mitigation technique and future work will be to explore the effects of refresh on the floating gate cells.
  - Discern failure mech.
- Rebound test, short term anneal

References

[1] S. Rezgui, J.J. Wang, E. Chan Tung, J. McCollum and B. Cronquist, "New Methodologies for SET Characterization and Mitigation in Flash-Based FPGAs", *IEEE TNS, Vol. 54, NO. 6,* Dec. 2007, pp 2512-2524.

[2] S. Rezgui, J.J. Wang, Y. Sun, B. Cronquist and J. McCollum, "New Reprogrammable and Non-Volatile Radiation Tolerant FPGA: RTA3P", *IEEE Aerospace 2008, Big Sky, MT, to be published at AIAA 2008.*

[3] S. Rezgui, J.J. Wang, Y. Sun, D. D'Silva, B. Cronquist and J. McCollum, "TID Characterization of 0.13 um Flash Based FPGAs" RADECS 2008, Finland.

[4] http://nepp.nasa.gov/

[5] http://parts.jpl.nasa.gov/

Appendix

- Part Lot/Date Codes
  - A3P600L-FGG484 0813 QH9P0
  - AGL600-FGG484 0801QH7R0091
  - A3P600-FGG484 0739 QH4H0